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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#3/105
10/17/2
Sullivan

Applicant: Yujiro KAJIHARA et al.

Serial No.: 09/989,242

Filed: 19 November 2001

For: LEAD FRAME SEMICONDUCTOR, INTEGRATED
CIRCUIT DEVICE USING THE SAME, AND METHOD
OF AND PROCESS FOR FABRICATING THE TWO

Group: Unassigned (Parent - 2815)

Examiner: Unassigned (Parent - J. Clark)

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

21 February 2002

Sir:

In the matter of the above-identified application, Applicant hereby submits the attached information for consideration by the Office under 37 C.F.R. §§1.97 and 1.98, as listed on the accompanying Form PTO-1449.

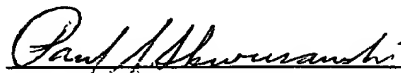
Applicant states that references listed on the attached Form PTO-1449 were first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement. Attached is a copy of a Korean Office Action citing the information. The date of the Korean Office Action, 21 November 2001, is noted in the upper left-hand corner and the lower middle of page 2-1, and the references are listed at the bottom of page 2-1.

No fee is required for the filing of this Statement because it is being submitted with the above-identified application filed concurrently herewith, as well as a statement of certification of filing within the three (3) month period following issuance

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of an Action in a corresponding foreign application. However, if any fees are actually proper for the filing of this paper, please charge same to ATS&K Deposit Account No. 01-2135 (as Order No. 501.32049RV2), and please credit any overpayment or excess fees thereto.

Respectfully submitted,



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ATTACHMENTS:

Korean Office Action of 11/21/01
Form PTO-1449
JP Publication No. 03-032048A
with English Abstract
JP Publication No. 02-094547A
with English Abstract

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